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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/663,025	WONG, JIA-FAM	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-20 and 26-38* is/are pending in the application.

4a) Of the above claim(s) *18-20,26-28 and 30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29,31-33,35 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/26/07 has been entered. An action on the RCE follows.

a. The amendment filed on 6/04/07 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claim 29 is rejected under 35 U.S.C. 102(e) as being anticipated by Na et al., US patent No. 5,942,767.

Regarding claims 29, Na teaches (fig. 5F) a thin film transistor (TFT), comprising: a gate electrode (12) with an island shape formed on a substrate (10); an insulating layer (14) covering the gate electrode (12); a semiconductor layer (16) with an island shape formed on the insulating layer (14), and positioned directly above the gate electrode (12); a source doped silicon layer (441 on the left) and a drain doped silicon

layer (441 on the right) formed on the semiconductor layer (16), a channel being defined between the source doped silicon layer and the drain doped silicon layer (region between the source/drain regions, 441) to expose the semiconductor layer therein (refer to fig. 5F); first and second sacrifice layers (461) with island shapes respectively formed on the source doped silicon layer (441 on the left) and drain doped silicon layer (441 on the right) and formed over the semiconductor layer (16), the first (461, on the left hand side of fig. 5F) and the second (441 on the right hand side of fig. 5F) sacrifice layers being spaced apart by the channel (region between source/drain) and further separated from the insulating layer (14) in their entirety, wherein an entire bottom of the first and second sacrifice layers (bottom surfaces of the first and second sacrifice layers 461) is higher than a top surface of the semiconductor layer (16); a source electrode (471) formed above the first sacrifice layer (461 on the left hand side), and the source dope silicon layer (441); and a drain electrode (471 on the right hand side) formed above the second sacrifice layer (461 on the right) and the drain doped silicon layer (441 on the right).

4. Claims 33 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimada et al., US patent No. 5,726,461.

Regarding claim 33, Shimada teaches (fig. 7) a thin film transistor (TFT), comprising: a gate electrode (11) with an island shape (refer to fig. 7) formed on a substrate (10); an insulating layer (12) covering the gate electrode (11); a semiconductor layer (13) with an island shape formed on the insulating layer (12), and

positioned above the gate electrode (11); first and second sacrifice layers (15) with island shapes formed over and in direct contact with the semiconductor layer (13) in their entirety, and a channel being defined between the first and second sacrifice layers (region between layer 15) so as to expose the semiconductor layer (13); a source doped silicon layer (25) and a drain doped silicon layer (25 on the right hand side) formed above the first sacrifice layer (15), second sacrifice layer (15 on the right hand side), and the semiconductor layer (13), the source doped silicon layer (25 on the left) and the drain doped silicon layer (25 on the right) being spaced apart by the channel (channel is formed between source/drain region), wherein the source doped silicon layer (25 on the left) and the drain doped silicon layer (25 on the right) are in contact (electrical contact) with the semiconductor layer; and a source electrode (16a) and a drain electrode (16b) respectively formed on the source doped silicon layer (25 on the left) and the drain doped silicon layer (25 on the right).

Regarding claim 35, Shimada teaches the entire claimed structure of claim 33 above including a passivation layer (17) covering the source electrode (16a), the drain electrode (16b), and the channel (region between source/drain).

The limitation that "the TFT is used in an in-plane-switch (IPS) type LCD" is not given patentable weight because a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative

difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). Furthermore the structure of Shimada can be used as in an in-plane-switch (IPS) type LCD.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable Na in view of Kaneko et al., US patent No., 6,433,842.

Regarding claim 31, Na teaches substantially the entire claimed structure of claim 29 above except explicitly stating that a passivation layer covering the source electrode, the drain electrode, and the channel, and the TFT is used in an in-plane switch (IPS) type LCD.

Kaneko teaches a passivation layer (10) covering the source electrode (9), the drain electrode (9), and the channel (region between source and drain region) and the channel, and the TFT is used in an in-plane switch (IPS) type LCD (col. 13, lines 57-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the passivation layer taught by Kaneko in the structure of Na in order to use it as a protection film for protecting the device from external pollution.

The limitation that "the TFT is used in an in-plane-switch (IPS) type LCD" is not given patentable weight because a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). Furthermore the structure Na as modified by Kaneko can be used as in an in-plane-switch (IPS) type LCD (col. 10, lines 51-61).

Regarding claim 32, Na teaches substantially the entire claimed structure of claim 29 above except explicitly stating that a passivation layer covering the TFT on the substrate, and having a hole above the drain electrode; and a transparent conductive layer formed above the drain electrode and electrically connected to the drain electrode via the hole.

Kaneko teaches a passivation layer (10) covering the TFT on the substrate (40), and having a hole (Kaneko, fig. 1) above the drain electrode (region where drain line 19 is formed, Kaneko, fig. 1); and a transparent conductive layer (11) formed above the drain electrode (9) and electrically connected to the drain electrode via the hole (refer to fig. 1, col. 9, lines 20-30, Kaneko).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the passivation layer covering the TFT on the

substrate, and having a hole above the drain electrode; and a transparent conductive layer formed above the drain electrode and electrically connected to the drain electrode via the hole as taught by Kaneko in the structure of Na in order provide a protection film for protecting the device from external pollution and ensure connection stability at the interconnection terminals and as a result improve the reliability of the device.

7. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada in view of Park et al., US patent No., 6,107,640.

Regarding claim 36, Shimada teaches substantially the entire claimed structure of claim 33 above except explicitly stating that a passivation layer covering the TFT on the substrate, and having a hole above the drain electrode; and a transparent conductive layer formed above the drain electrode and electrically connected to the drain electrode via the hole.

Park teaches a passivation layer (47) covering the TFT on the substrate (31), and having a hole (49) above the drain electrode (45); and a transparent conductive layer (51) formed above the drain electrode (45) and electrically connected to the drain electrode (45) via the hole (refer to fig. 2D).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the hole above the drain electrode and a transparent conductive layer formed above the drain electrode and electrically connected to the drain electrode via the hole as taught by Park in the structure of Shimada in order to

form a thin film transistor with improved prevention against the formation of native oxide (col. 1, lines 6-15).

Response to Arguments

8. Applicant's arguments with respect to claims 29 and 31-32 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with regards to claims 33 and 35-36 filed 6/04/07 have been fully considered but they are not persuasive. Applicant argues that Shimada does teach that the n+ amorphous silicon layer (25) does not contact the semiconductor layer (13). However Shimada teaches that the source doped silicon layer (25 on the left) and the drain doped silicon layer (25 on the right) are in contact (electrical contact) with the semiconductor layer as claimed.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571)-272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SAMUEL ADMASSU GEBREMARIAM
SAG
August 20, 2007